EXPRESS MAIL NO. EL863782889US

WHAT IS CLAIMED IS:

1. A differential data sampling circuit comprising:

a latch circuit for sampling a differential data signal in response to a first strobe signal; and

a strobe circuit coupled to the latch circuit, the strobe circuit capturing the output of the latch circuit based on a second strobe signal.

2. The differential data sampling circuit according to claim 1, wherein the latch circuit produces a voltage change at output that is less than the voltage difference between a power supply voltage that supplies the latch circuit and ground.

3. The differential data sampling circuit according to claim 1,

wherein the latch circuit is an analog latch circuit that latches the differential data signal in response to the first strobe signal so as to produce a latched voltage, and

the strobe circuit samples and holds the latched voltage in order to determine a logic level of the differential data signal.

4. The differential data sampling circuit according to claim 1, wherein the first strobe signal is delayed to produce the second strobe signal.

5. The differential data sampling circuit according to claim 1, wherein the first strobe signal and the second strobe signal are the same signal.

6. The differential data sampling circuit according to claim 1, wherein the latch circuit includes load elements, and each of the load elements includes a diode-connected transistor.

7. The differential data sampling circuit according to claim 1, wherein the latch circuit includes:

an input branch and a latch branch connected in parallel; and

a bias current control transistor coupled in series with both the input branch and the latch branch.

8. The differential data sampling circuit according to claim 7, wherein the input branch of the latch circuit includes:

a pair of differential input transistors; and

a single strobe transistor coupled in series with the pair of differential input transistors.

9. The differential data sampling circuit according to claim 1, wherein the latch circuit receives only one bias voltage.

10. The differential data sampling circuit according to claim 1, further comprising a high speed differential buffer having an output coupled to the input of the latch circuit, the high speed differential buffer receiving a differential input signal.

11. The differential data sampling circuit according to claim 10, wherein the differential input signal received by the high speed differential buffer is composed of a single input data signal and a reference voltage.

12. A digital data receiver including at least one differential data sampling circuit, said differential data sampling circuit comprising:

a latch circuit for sampling a differential data signal in response to a first strobe signal; and

a strobe circuit coupled to the latch circuit, the strobe circuit capturing the output of the latch circuit based on a second strobe signal.

13. The digital data receiver according to claim 12, wherein the latch circuit produces a voltage change at output that is less than the voltage difference between a power supply voltage that supplies the latch circuit and ground.

14. The digital data receiver according to claim 12,

wherein the latch circuit is an analog latch circuit that latches the differential data signal in response to the first strobe signal so as to produce a latched voltage, and

the strobe circuit samples and holds the latched voltage in order to determine a logic level of the differential data signal.

15. The digital data receiver according to claim 12, wherein the first strobe signal is delayed to produce the second strobe signal.

16. The digital data receiver according to claim 12, wherein the latch circuit includes:

an input branch and a latch branch connected in parallel; and

a bias current control transistor coupled in series with both the input branch and the latch branch.

17. The digital data receiver according to claim 16, wherein the input branch of the latch circuit includes:

a pair of differential input transistors; and

a single strobe transistor coupled in series with the pair of differential input transistors.

18. The digital data receiver according to claim 12, wherein the latch circuit receives only one bias voltage.

19. The digital data receiver according to claim 12, wherein the differential data sampling circuit further includes a high speed differential buffer having an output coupled to the input of the latch circuit, the high speed differential buffer receiving a differential input signal.

20. The digital data receiver according to claim 19, wherein the differential input signal received by the high speed differential buffer is composed of a single input data signal and a reference voltage.